ESP32-H2-MINI-1
ESP32-H2-MINI-1U

Datasheet Version 1.2

Bluetooth® Low Energy and IEEE 802.15.4 module
Built around ESP32-H2 series of SoCs, RISC-V single-core 32-bit microprocessor
2 MB or 4 MB flash in chip package
19 GPIOs
On-board PCB antenna or external antenna connector

ESP32-H2-MINI-1

ESP32-H2-MINI-1U

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-h2-mini-1_mini-1u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-H2 embedded, RISC-V single-core 32-bit microprocessor, up to 96 MHz
- 128 KB ROM
- 320 KB SRAM
- 4 KB LP Memory
- 2 MB or 4 MB in-package flash

Bluetooth®

- Bluetooth Low Energy (Bluetooth 5.3 certified)
- Bluetooth mesh
- Bluetooth Low Energy long range (Coded PHY, 125 Kbps and 500 Kbps)
- Bluetooth Low Energy high speed (2 Mbps)
- Bluetooth Low Energy advertising extensions and multiple advertising sets
- Simultaneous operation of Broadcaster, Observer, Central, and Peripheral devices
- Multiple connections
- LE power control

IEEE 802.15.4

- IEEE Standard 802.15.4-2015 compliant
- Supports 250 Kbps data rate in 2.4 GHz band and OQPSK PHY
- Supports Thread
- Supports Zigbee 3.0
- Supports Matter
- Supports other application-layer protocols (HomeKit, MQTT, etc)

Peripherals

- Up to 19 GPIOs
  - 3 strapping pins
- I2C, I2S, SPI, UART, ADC, LED PWM, ETM, GDMA, PCNT, PARLIO, RMT, TWAI®, MCPWM, USB Serial/JTAG, temperature sensor, general-purpose timers, system timer, watchdog timer

Integrated Components on Module

- 32 MHz crystal oscillator

Antenna Options

- ESP32-H2-MINI-1: On-board PCB antenna
- ESP32-H2-MINI-1U: External antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0~3.6 V
- Operating ambient temperature: 40~105 °C

Certification

- RF certification: See certificates

1.2 Series Comparison

ESP32-H2-MINI-1 and ESP32-H2-MINI-1U are two powerful, generic Bluetooth® Low Energy and IEEE 802.15.4 combo module that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios related to Internet of Things (IoT), such as embedded systems, smart home, wearable electronics, etc.

ESP32-H2-MINI-1 comes with a PCB antenna. ESP32-H2-MINI-1U comes with a connector for an external antenna.

The series comparison for the two modules is as follows:

Table 1: ESP32-H2-MINI-1 Series Comparison [1]

Ordering Code	Flash [4]	Ambient Temp. [2] (°C)	Size [3] (mm)
ESP32-H2-MINI-1-H2S	2 MB (Quad SPI)	−40∼105	13.2 × 16.6 × 2.4
ESP32-H2-MINI-1-H4S	4 MB (Quad SPI)	−40∼105	

[1] This table shares the same notes presented in Table 2 below.

Table 2: ESP32-H2-MINI-1U Series Comparison

Ordering Code	Flash [4]	Ambient Temp. [2] (°C)	Size [3] (mm)
ESP32-H2-MINI-1U-H2S	2 MB (Quad SPI)	−40∼105	13.2 × 12.5 × 2.4
ESP32-H2-MINI-1U-H4S	4 MB (Quad SPI)	−40∼105	

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[3] For details, refer to Section 10.1 *Module Dimensions*.

[4] The flash is integrated in the chip's package. The flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

At the core of this module is ESP32-H2, a 32-bit RISC-V single-core CPU that operates at up to 96 MHz.

Note:
* For more information on ESP32-H2, please refer to *ESP32-H2 Series Datasheet*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- Matter Solutions
- Wearables
- Service Robot
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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2 Block Diagram

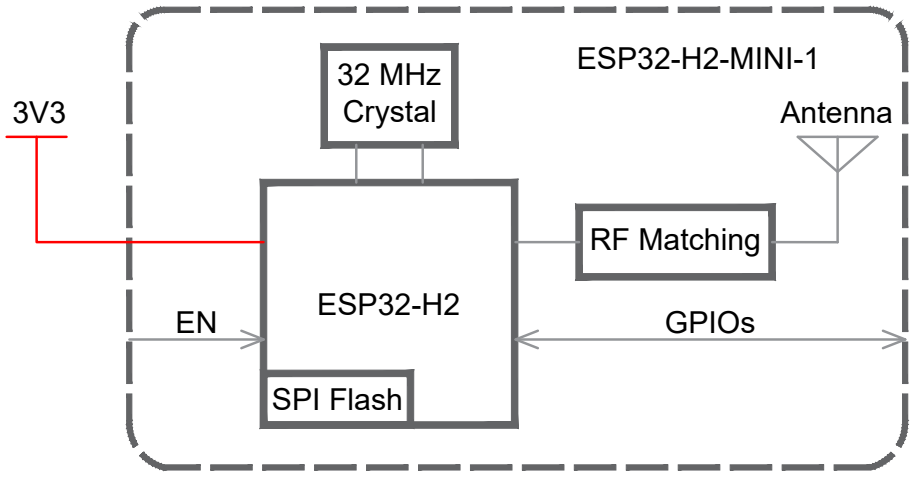

Figure 1: ESP32-H2-MINI-1 Block Diagram

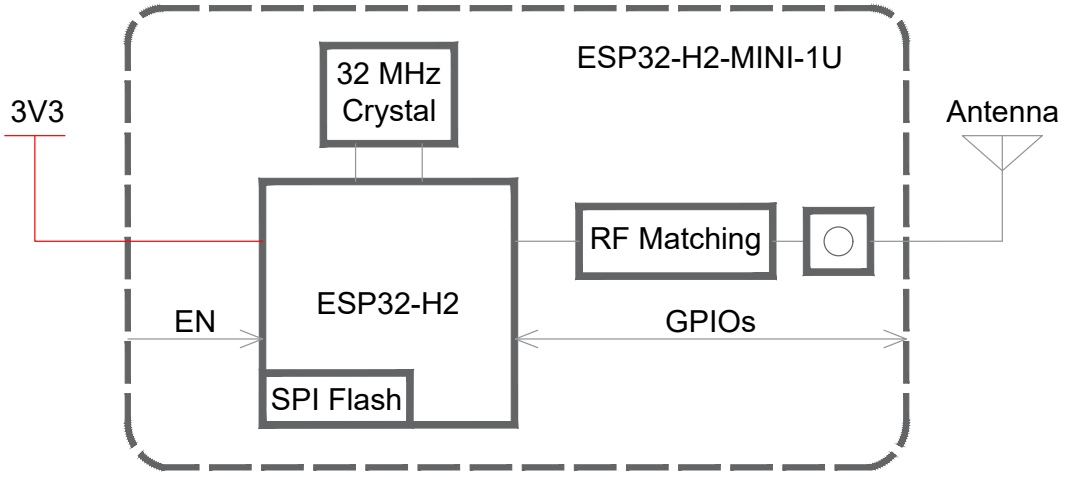

Figure 2: ESP32-H2-MINI-1U Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Module Dimensions*.

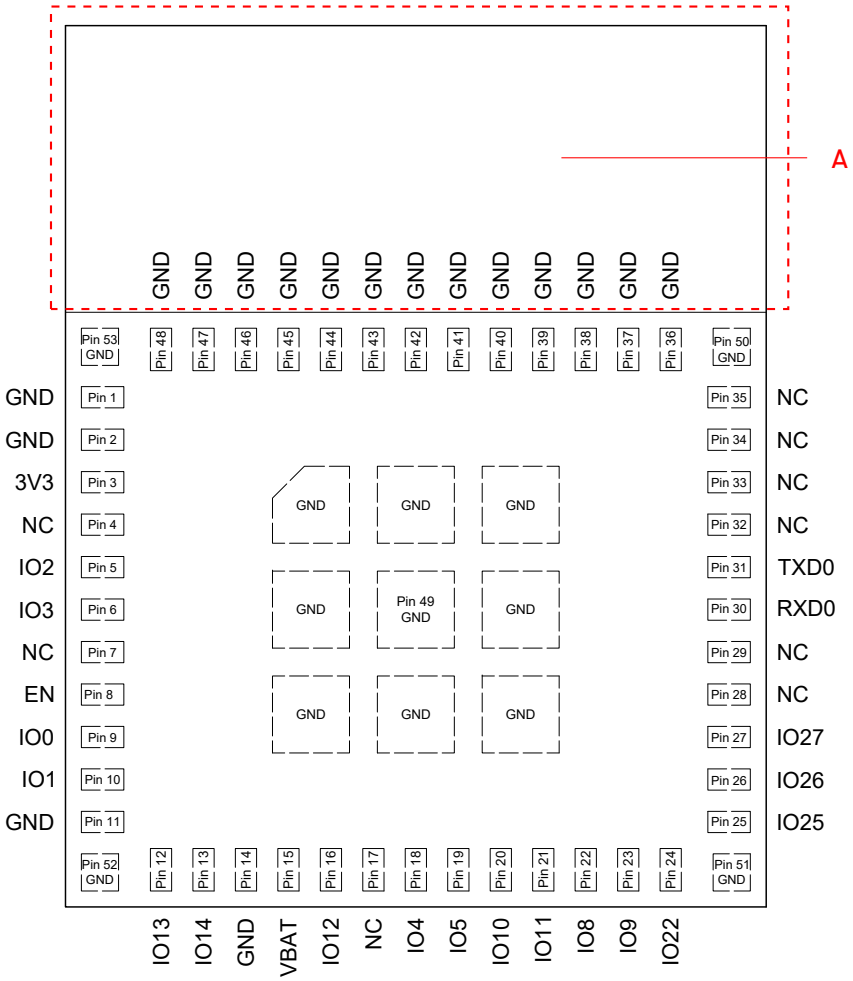

Figure 3: Pin Layout (Top View)

Note A:
The zone marked with dotted lines is the antenna keepout zone. The pin diagram is applicable to ESP32-H2-MINI-1 and ESP32-H2-MINI-1U, but the latter has no antenna keepout zone.
To learn more about the keepout zone for module's antenna on the base board, please refer to *ESP32-H2 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

3.2 Pin Description

The module has 53 pins. See pin definitions in Table 3 *Pin Description*.

For peripheral pin configurations, please refer to *ESP32-H2 Series Datasheet*.

Table 3: Pin Definitions

Name	No.	Type[1]	Function
GND	1, 2, 11, 14, 36~53	P	Ground
3V3	3	P	Power supply
NC	4, 7, 17, 28, 29, 32~35	—	NC
IO2	5	I/O/T	GPIO2, FSPIWP, ADC1_CH1, **MTMS**
IO3	6	I/O/T	GPIO3, FSPIHD, ADC1_CH2, **MTDO**
EN	8	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO0	9	I/O/T	**GPIO0**, FSPIQ
IO1	10	I/O/T	**GPIO1**, FSPICS0, ADC1_CH0
GND	11	P	Ground
IO13	12	I/O/T	**GPIO13**, XTAL_32K_P
IO14	13	I/O/T	**GPIO14**, XTAL_32K_N
GND	14	P	Ground
VBAT	15	P	Connected to internal 3V3 power supply (Default) or external battery power supply (3.0 ~ 3.6 V).
IO12	16	I/O/T	**GPIO12**
IO4	18	I/O/T	GPIO4, FSPICLK, ADC1_CH3, **MTCK**
IO5	19	I/O/T	GPIO5, FSPID, ADC1_CH4, **MTDI**
IO10	20	I/O/T	**GPIO10**, ZCD0
IO11	21	I/O/T	**GPIO11**, ZCD1
IO8	22	I/O/T	**GPIO8**
IO9	23	I/O/T	**GPIO9**
IO22	24	I/O/T	**GPIO22**
IO25	25	I/O/T	**GPIO25**, FSPICS3
IO26	26	I/O/T	GPIO26, FSPICS4, **USB_D-**
IO27	27	I/O/T	GPIO27, FSPICS5, **USB_D+**
RXD0	30	I/O/T	GPIO23, FSPICS1, **U0RXD**
TXD0	31	I/O/T	GPIO24, FSPICS2, **U0TXD**

[1] P: power supply; I: input; O: output; T: high impedance.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-H2 Series Datasheet* > Section *Boot Configurations via Strapping Pins and eFuses*. For the strapping pin mapping between the chip and modules, please refer to Chapter 10 *Physical Dimensions*.

The chip allows for configuring the following boot parameters through strapping pins, eFuse bits, and registers at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO8 and GPIO9
- **ROM message printing**
  - Strapping pin: GPIO8
  - eFuse bits: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
  - Register: LP_AON_STORE4_REG[0]
- **JTAG signal source**
  - Strapping pin: GPIO25
  - eFuse bits: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse bits are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once an eFuse bit is programmed to 1, it can never be reverted to 0. For how to program eFuse bits, please refer to *ESP32-H2 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO8	Floating	—
GPIO9	Weak pull-up	1
GPIO25	Floating	—

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-H2 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 5 and Figure 4.

Table 5: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_EN pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_EN is already high and before these pins start operating as regular IO pins.	3

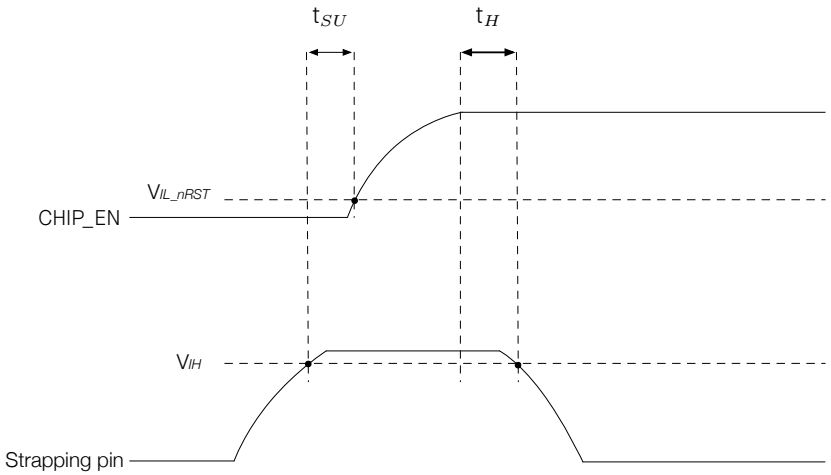

Figure 4: Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 6 *Chip Boot Mode Control*.

Table 6: Chip Boot Mode Control

Boot Mode [1]	GPIO8	GPIO9
SPI Boot	Any value	**1**
Joint Download Boot [2]	1	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB Download Boot:
  - USB-Serial-JTAG Download Boot
- UART Download Boot

4.2 ROM Messages Printing Control

During the boot process, ROM message printing is enabled if LP_AON_STORE4_REG[0] is 0 (default), and disabled if LP_AON_STORE4_REG[0] is 1. When ROM message printing is enabled, the messages can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL, LP_AON_STORE4_REG[0], and GPIO8 control ROM messages printing to **UART0** as shown in Table 7 *UART0 ROM Message Printing Control*.

Table 7: UART0 ROM Message Printing Control

UART0 ROM Message Printing [1]	LP_AON_STORE4_REG[0]	EFUSE_UART_PRINT_CONTROL	GPIO8
Enabled	**0**	**0**	Ignored
		1	0
		2	1
Disabled	0	1	1
		2	0
		3	Ignored
	1	Ignored	Ignored

[1] **Bold** marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to **USB Serial/JTAG controller** as shown in Table 8 *USB Serial/JTAG ROM Message Printing Control*.

Table 8: USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Message Printing Control [1]	LP_AON_STORE4_REG[0]	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled	**0**	**0**
Disabled	0	1
	1	Ignored

[1] **Bold** marks the default value and configuration.

4.3 JTAG Signal Source Control

The strapping pin GPIO25 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 9 shows GPIO25 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

Table 9: JTAG Signal Source Control

JTAG Signal Source [1]	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_STRAP_JTAG_SEL_ENABLE	GPIO25
USB Serial/JTAG Controller	**0**	**0**	**0**	Ignored
JTAG pins [2]			1	0
USB Serial/JTAG Controller				1
JTAG pins [2]	0	1	Ignored	Ignored
USB Serial/JTAG Controller	1	0	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

[1] **Bold** marks the default value and configuration.

[2] JTAG pins refer to MTDI, MTCK, MTMS, and MTDO.

5 Peripherals

5.1 Peripheral Overview

ESP32-H2 integrates a rich set of peripherals including SPI, I2S, UART, I2C, LED PWM, ADC, TWAI®, temperature sensor, etc.

To learn more about on-chip components, please refer to *ESP32-H2 Series Datasheet* > Section *Functional Description*.

Note:
The content below is sourced from *ESP32-H2 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-H2-MINI-1 and ESP32-H2-MINI-1U as not all the IO signals are exposed on the module.
To learn more about peripheral signals, please refer to *ESP32-H2 Technical Reference Manual* > Section *Peripheral Signal List*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interfaces

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

The UART Controller in the ESP32-H2 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It consists of two UARTs in the system.

Feature List

- Programmable baud rates up to 5 MBaud
- 260 x 8 bit RAM shared by TX FIFOs and RX FIFOs
- Support for various lengths of data bits and stop bits
- Parity bit support
- Special character AT_CMD detection
- RS485 protocol support
- IrDA protocol support
- High-speed data communication using GDMA
- Receive timeout feature
- UART as the wake-up source

- Software and hardware flow control

Pin Assignment

The pins connected to receive and transmit signals (U0RXD and U0TXD) for **UART0** are multiplexed with GPIO23 ~ GPIO24 and FSPICS1 ~ FSPICS2 via IO MUX. Other signals can be routed to any GPIOs via the GPIO matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.2 SPI Controller

ESP32-H2 has the following SPI interfaces:

- **SPI0/SPI1** are reserved for system use.
- **SPI2** is a general-purpose SPI (GP-SPI) controller with access to general-purpose DMA channels.

Features of SPI2

- Supports operation as a master or slave
- Support for DMA
- Supports Single SPI, Dual SPI, Quad SPI, QPI modes
- Configurable clock polarity (CPOL) and phase (CPHA)
- Configurable clock frequency
- Data transmission is in bytes
- Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
- As a master
  - Supports 2-line full-duplex communication with clock frequency up to 48 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 48 MHz
  - Provides six FSPICS... pins for connection with six independent SPI slaves
  - Configurable CS setup time and hold time
- As a slave
  - Supports 2-line full-duplex communication with clock frequency up to 32 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 32 MHz

Pin Assignment

- Via IO MUX
  For SPI2, the pins for data and clock signals are multiplexed with GPIO0, GPIO2 ~ GPIO5, and JTAG interface via the IO MUX. The pins for chip select signals are multiplexed with GPIO1, GPIO23 ~ GPIO27, UART0 interface, and USB interface via the IO MUX.

- Via GPIO Matrix
  The pins for SPI2 can be chosen from any GPIOs via the GPIO matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.3 I2C Controller

The I2C Controller supports communication between the master and slave devices using the I2C bus.

Feature List

- Two I2C controllers
- Communication with multiple external devices
- Master and slave modes
- Standard mode (100 Kbit/s) and fast mode (400 Kbit/s)
- SCL clock stretching in slave mode
- Programmable digital noise filtering
- Support for 7-bit and 10-bit addressing, as well as dual address mode

Pin Assignment

The pins used for I2C can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.4 I2S Controller

The I2S Controller in the ESP32-H2 chip provides a flexible communication interface for streaming digital data in multimedia applications, particularly digital audio applications.

Feature List

- Master mode and slave mode
- Full-duplex and half-duplex communications
- Separate TX and RX units that can work independently or simultaneously
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- PCM-to-PDM TX interface

- Configurable high-precision BCK clock, with frequency up to 40 MHz
  - Sampling frequencies can be 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 128 kHz, etc.
- 8-/16-/24-/32-bit data communication
- Direct Memory Access (DMA)
- A-law and μ-law compression/decompression algorithms for improved signal-to-quantization noise ratio
- Flexible data format control

Pin Assignment

The pins for the I2S Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.5 Pulse Count Controller

The Pulse Count Controller (PCNT) is designed to count input pulses by tracking the rising and falling edges of the input pulse signal.

Feature List

- Four independent pulse counters with two channels each
- Counter modes: increment, decrement, or disable
- Glitch filtering for input pulse signals and control signals
- Selection between counting on rising or falling edges of the input pulse signal

Pin Assignment

The pins for the Pulse Count Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.6 USB Serial/JTAG Controller

The USB Serial/JTAG controller in the ESP32-H2 chip provides an integrated solution for communicating to the chip over a standard USB CDC-ACM serial port as well as a convenient method for JTAG debugging. It eliminates the need for external chips or JTAG adapters, saving space and reducing cost.

Feature List

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- CDC-ACM virtual serial port and JTAG adapter functionality
- CDC-ACM:

  - CDC-ACM adherent serial port emulation (plug-and-play on most modern OSes)
  - Host controllable chip reset and entry into download mode
- JTAG adapter functionality:
  - Fast communication with CPU debugging core using a compact representation of JTAG instructions
- Internal PHY

Pin Assignment

The pins USB_D+ and USB_D- for the USB Serial/JTAG Controller are multiplexed with GPIO26 ~ GPIO27 and FSPICS4 ~ FSPICS5 via IO MUX.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.7 Two-wire Automotive Interface

The Two-wire Automotive Interface (TWAI®) is a multi-master, multi-cast communication protocol designed for automotive applications. The TWAI controller facilitates the communication based on this protocol.

Feature List

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- Special transmissions: Single-shot and Self Reception
- Acceptance filter (single and dual filter modes)
- Error detection and handling: error counters, configurable error warning limit, error code capture, arbitration lost capture, automatic transceiver standby

Pin Assignment

The pins for the Two-wire Automotive Interface can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.8 LED PWM Controller

The LED PWM Controller (LEDC) is designed to generate PWM signals for LED control.

Feature List

- Six independent PWM generators
- Maximum PWM duty cycle resolution of 20 bits

- Four independent timers with 20-bit counters, configurable fractional clock dividers and counter overflow values
- Adjustable phase of PWM signal output
- PWM duty cycle dithering
- Automatic duty cycle fading
  - Linear duty cycle fading — only one duty cycle range
  - Gamma curve fading — up to 16 duty cycle ranges for each PWM generator, with independently configured fading direction (increase or decrease), fading amount, number of fades, and fading frequency
- PWM signal output in low-power mode (Light-sleep mode)
- Event generation and task response achieved by the Event Task Matrix (ETM)

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.9 Motor Control PWM

The Motor Control Pulse Width Modulator (MCPWM) is designed for driving digital motors and smart light. The MCPWM is divided into five main modules: PWM timers, PWM operators, Capture module, Fault Detection module, and Event Task Matrix (ETM) module.

Feature List

- Three PWM timers for precise timing and frequency control
  - Every PWM timer has a dedicated 8-bit clock prescaler
  - The 16-bit counter in the PWM timer can work in count-up mode, count-down mode, or count-up-down mode
  - Hardware or software synchronization to trigger a reload on the PWM timer or the prescaler's restart, with selectable hardware synchronization source
- Three PWM operators for generating waveform pairs
  - Six PWM outputs to operate in several topologies
  - The control of the PWM signal can be updated asynchronously
  - Configurable dead time on rising and falling edges; each set up independently
  - Modulating of PWM output by high-frequency carrier signals, useful when gate drivers are insulated with a transformer
  - Period, time stamps, and important control registers have shadow registers with flexible updating methods

- Capture module for hardware-based signal processing
  - Speed measurement of rotating machinery
  - Measurement of elapsed time between position sensor pulses
  - Period and duty cycle measurement of pulse train signals
  - Decoding current or voltage amplitude derived from duty-cycle-encoded signals of current/voltage sensors
  - Three individual capture channels, each of which with a 32-bit time-stamp register
  - Selection of edge polarity and prescaling of input capture signals
  - The capture timer can sync with a PWM timer or external signals
- Fault Detection module
  - Programmable fault handling in both cycle-by-cycle mode and one-shot mode
  - A fault condition can force the PWM output to either high or low logic levels
- Event generation and task response achieved by the Event Task Matrix (ETM)

Pin Assignment

The pins for the Motor Control PWM can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.10 Remote Control Peripheral

The Remote Control Peripheral (RMT) controls the transmission and reception of infrared remote control signals.

Feature List

- Four channels for sending and receiving infrared remote control signals
- Independent transmission and reception capabilities for each channel
- Support for Normal TX/RX mode, Wrap TX/RX mode, Continuous TX mode
- Modulation on TX pulses and Demodulation on RX pulses
- RX filtering for improved signal reception
- Ability to transmit data simultaneously on multiple channels
- Clock divider counter, state machine, and transmitter for each TX channel
- Clock divider counter, state machine, and receiver for each RX channel
- Default allocation of RAM blocks to channels based on channel number
- RAM containing 16-bit entries with “level” and “period” fields

Pin Assignment

The pins for the Remote Control Peripheral can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.11 Parallel IO Controller

The Parallel IO Controller (PARLIO) in the ESP32-H2 chip enables data transfer between external devices and internal memory on a parallel bus through GDMA. It consists of a transmitter (TX unit) and a receiver (RX unit), making it a versatile interface for connecting various peripherals.

Feature List

- 1/2/4/8-bit configurable data bus width
- Full-duplex communication with 8-bit data bus width
- Bit reordering in 1/2/4-bit data bus width mode
- RX unit supports eight receive modes categorized into three major categories: Level Enable mode, Pulse Enable mode, and Software Enable mode
- TX unit can generate a valid signal aligned with TXD

Pin Assignment

The pins for the Parallel IO Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 SAR ADC

ESP32-H2 integrates a Successive Approximation Analog-to-Digital Converter (SAR ADC) to convert analog signals into digital representations.

Feature List

- 12-bit sampling resolution
- Analog voltage sampling from up to five pins
- Attenuation of input signals for voltage conversion
- Software-triggered one-time sampling
- Timer-triggered multi-channel scanning
- DMA continuous conversion for seamless data transfer

- Two filters with configurable filter coefficient
- Threshold monitoring which helps to trigger an interrupt
- Support for Event Task Matrix

Pin Assignment

The pins for the SAR ADC are multiplexed with GPIO0 ~ GPIO5, JTAG interface, and SPI2 interface.

For more information about the pin assignment, see *ESP32-H2 Series Datasheet* > Section *IO Pins* and *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2.2 Temperature Sensor

The Temperature Sensor in the ESP32-H2 chip allows for real-time monitoring of temperature changes inside the chip.

Feature List

- Measurement range: −40°C ~ 125°C
- Software triggering, wherein the data can be read continuously once triggered
- Hardware automatic triggering and temperature monitoring
- Configurable temperature offset based on the environment to improve the accuracy
- Adjustable measurement range
- Two automatic monitoring wake-up modes: absolute value mode and incremental value mode
- Support for Event Task Matrix

5.2.2.3 Analog PAD Voltage Comparator

ESP32-H2 integrates two analog voltage comparators. These comparators rely on special pads that support voltage comparison functionality to monitor voltage changes on these pads. Each analog voltage comparator has two pads associated with it, for the main voltage and the reference voltage respectively. The voltage comparison result generated by the analog voltage comparator can be used as Event Task Matrix (ETM) events to drive ETM tasks of other peripherals or trigger interrupts.

Feature List

- Voltage comparison
  - Configurable voltage comparison mode
  - Configurable reference voltage
- Interrupt upon changes of voltage comparison result
- ETM event generation

Pin Assignment

The pins for the analog voltage pad comparators are multiplexed with GPIO10 ~ GPIO11.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 10 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 11 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 10: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	105	°C

6.2 Recommended Operating Conditions

Table 11: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	−40	—	105	°C

6.3 DC Characteristics (3.3 V, 25 °C)

Table 12: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage	−0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 13: Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 18.0 dBm	112
		Bluetooth LE @ 7.0 dBm	55
		Bluetooth LE @ −2.0 dBm	35
		Bluetooth LE @ −24.0 dBm	26
	RX	Bluetooth LE	25

Table 14: Current Consumption for 802.15.4 in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.15.4 @ 18.0 dBm	123
		802.15.4 @ 7.0 dBm	54
		802.15.4 @ −2.0 dBm	38
		802.15.4 @ −22.0 dBm	28
	RX	802.15.4	29

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-H2 Series Datasheet*.

6.4.2 Current Consumption in Other Modes

The measurements below are applicable to ESP32-H2FH2S and ESP32-H2FH4S.

Table 15: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ [1] (mA) All Peripheral Clocks Disabled	Typ [1] (mA) All Peripheral Clocks Enabled
Modem-sleep [2]	96	CPU running	10	17
		CPU in idle	6	13
	64	CPU running	8	13
		CPU in idle	5	10
	48	CPU running	7	11
		CPU in idle	5	9
	32	CPU running	4	8
		CPU in idle	3	7

[1] In practice, the current consumption might be different depending on which peripherals are enabled.
[2] In Modem-sleep mode, the current consumption might be higher when accessing flash.

Table 16: Current Consumption in Low-Power Modes

Work mode	Description	Typ (μA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	85
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	25
Deep-sleep	LP timer and LP memory are powered on	7
Power off	CHIP_EN is set to low level, the chip is powered off	1

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance
of 50 Ω.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 Bluetooth 5 (LE) Radio

Table 17: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402∼2480 MHz
RF transmit power range	−24∼20 dBm

7.1.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 18: Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	2.3	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.3	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.6	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.5	—	kHz
Modulation characteristics	$\Delta\ F1_{avg}$	—	250.3	—	kHz
	Min. $\Delta\ F2_{max}$ (for at least 99.9% of all $\Delta\ F2_{max}$)	—	216.3	—	kHz
	$\Delta\ F2_{avg}/\Delta\ F1_{avg}$	—	0.91	—	—
In-band emissions	± 2 MHz offset	—	−30	—	dBm
	± 3 MHz offset	—	−34	—	dBm
	> ± 3 MHz offset	—	−36	—	dBm

Table 19: Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	4.7	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.4	—	kHz

Cont'd on next page

Table 19 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	–	1.4	–	kHz
	$\lvert f_1 - f_0 \rvert$	–	0.6	–	kHz
Modulation characteristics	$\Delta\ F1_{\text{avg}}$	–	502.5	–	kHz
	Min. $\Delta\ F2_{\text{max}}$ (for at least 99.9% of all $\Delta\ F2_{\text{max}}$)	–	491.8	–	kHz
	$\Delta\ F2_{\text{avg}}/\Delta\ F1_{\text{avg}}$	–	0.90	–	–
In-band emissions	± 4 MHz offset	–	–32	–	dBm
	± 5 MHz offset	–	–33	–	dBm
	> ± 5 MHz offset	–	–36	–	dBm

Table 20: Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	1.5	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	1.0	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	1.4	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	1.2	–	kHz
Modulation characteristics	$\Delta\ F1_{\text{avg}}$	–	251.5	–	kHz
	Min. $\Delta\ F1_{\text{max}}$ (for at least 99.9% of all $\Delta\ F1_{\text{max}}$)	–	241.4	–	kHz
In-band emissions	± 2 MHz offset	–	–36	–	dBm
	± 3 MHz offset	–	–43	–	dBm
	> ± 3 MHz offset	–	–43	–	dBm

Table 21: Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	2.5	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	0.8	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.3	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	1.2	–	kHz
Modulation characteristics	$\Delta\ F2_{\text{avg}}$	–	231.7	–	kHz
	Min. $\Delta\ F2_{\text{max}}$ (for at least 99.9% of all $\Delta\ F2_{\text{max}}$)	–	220.0	–	kHz
In-band emissions	± 2 MHz offset	–	–30	–	dBm
	± 3 MHz offset	–	–34	–	dBm
	> ± 3 MHz offset	–	–37	–	dBm

Note that the In-band emissions in Table 18 and Table 21 above are tested at 15 dBm of TX power. However, the test result still meets the Bluetooth SIG standard even if the TX power is increased up to 20 dBm.

7.1.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 22: Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–98.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	2	—	dB
		F = F0 – 1 MHz	—	0	—	dB
		F = F0 + 2 MHz	—	–29	—	dB
		F = F0 – 2 MHz	—	–29	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–36	—	dB
		F ≥ F0 + 4 MHz	—	–30	—	dB
		F ≤ F0 – 4 MHz	—	–36	—	dB
	Image frequency	—	—	–30	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–32	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–16	—	dBm
		2003 MHz ~ 2399 MHz	—	–12	—	dBm
		2484 MHz ~ 2997 MHz	—	–16	—	dBm
		3000 MHz ~ 12.75 GHz	—	0	—	dBm
Intermodulation		—	—	–35	—	dBm

Table 23: Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–95.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	5	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	1	—	dB
		F = F0 – 2 MHz	—	–2	—	dB
		F = F0 + 4 MHz	—	–27	—	dB
		F = F0 – 4 MHz	—	–32	—	dB
		F = F0 + 6 MHz	—	–33	—	dB
		F = F0 – 6 MHz	—	–36	—	dB
		F ≥ F0 + 8 MHz	—	–36	—	dB
		F ≤ F0 – 8 MHz	—	–36	—	dB
	Image frequency	—	—	–26	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–33	—	dB
		F = F_{image} – 2 MHz	—	1	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–17	—	dBm
		2003 MHz ~ 2399 MHz	—	–27	—	dBm
		2484 MHz ~ 2997 MHz	—	–17	—	dBm

Cont'd on next page

Table 23 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	3000 MHz ~ 12.75 GHz	—	0	—	dBm
Intermodulation	—	—	–27	—	dBm

Table 24: Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–105.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	0	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–4	—	dB
		F = F0 – 1 MHz	—	–6	—	dB
		F = F0 + 2 MHz	—	–31	—	dB
		F = F0 – 2 MHz	—	–34	—	dB
		F = F0 + 3 MHz	—	–39	—	dB
		F = F0 – 3 MHz	—	–48	—	dB
		F $\geq$ F0 + 4 MHz	—	–35	—	dB
		F $\leq$ F0 – 4 MHz	—	–48	—	dB
	Image frequency	—	—	–39	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–38	—	dB
		F = F_{image} – 1 MHz	—	–39	—	dB

Table 25: Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–101.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	2	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–1	—	dB
		F = F0 – 1 MHz	—	–4	—	dB
		F = F0 + 2 MHz	—	–28	—	dB
		F = F0 – 2 MHz	—	–29	—	dB
		F = F0 + 3 MHz	—	–38	—	dB
		F = F0 – 3 MHz	—	–41	—	dB
		F $\geq$ F0 + 4 MHz	—	–33	—	dB
		F $\leq$ F0 – 4 MHz	—	–41	—	dB
	Image frequency	—	—	–33	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–38	—	dB

7.2 802.15.4 Radio

Table 26: 802.15.4 RF Characteristics

Name	Description
Center frequency range of operating channel	2405~2480 MHz

[1] Zigbee in the 2.4 GHz range supports 16 channels at 5 MHz spacing from channel 11 to channel 26.

7.2.1 802.15.4 RF Transmitter (TX) Characteristics

Table 27: 802.15.4 Transmitter Characteristics - 250 Kbps

Parameter	Min	Typ	Max	Unit
RF transmit power range	-24	—	20	dBm
EVM	—	3.8%	—	—

7.2.2 802.15.4 RF Receiver (RX) Characteristics

Table 28: 802.15.4 Receiver Characteristics - 250 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @1% PER		—	—	-101.5	—	dBm
Maximum received signal @1% PER		—	—	8	—	dBm
Relative jamming level	Adjacent channel	F = F0 + 5 MHz	—	31	—	dB
		F = F0 - 5 MHz	—	43	—	dB
	Alternate channel	F = F0 + 10 MHz	—	49	—	dB
		F = F0 - 10 MHz	—	54	—	dB

8 Module Schematics

This is the reference design of the module.

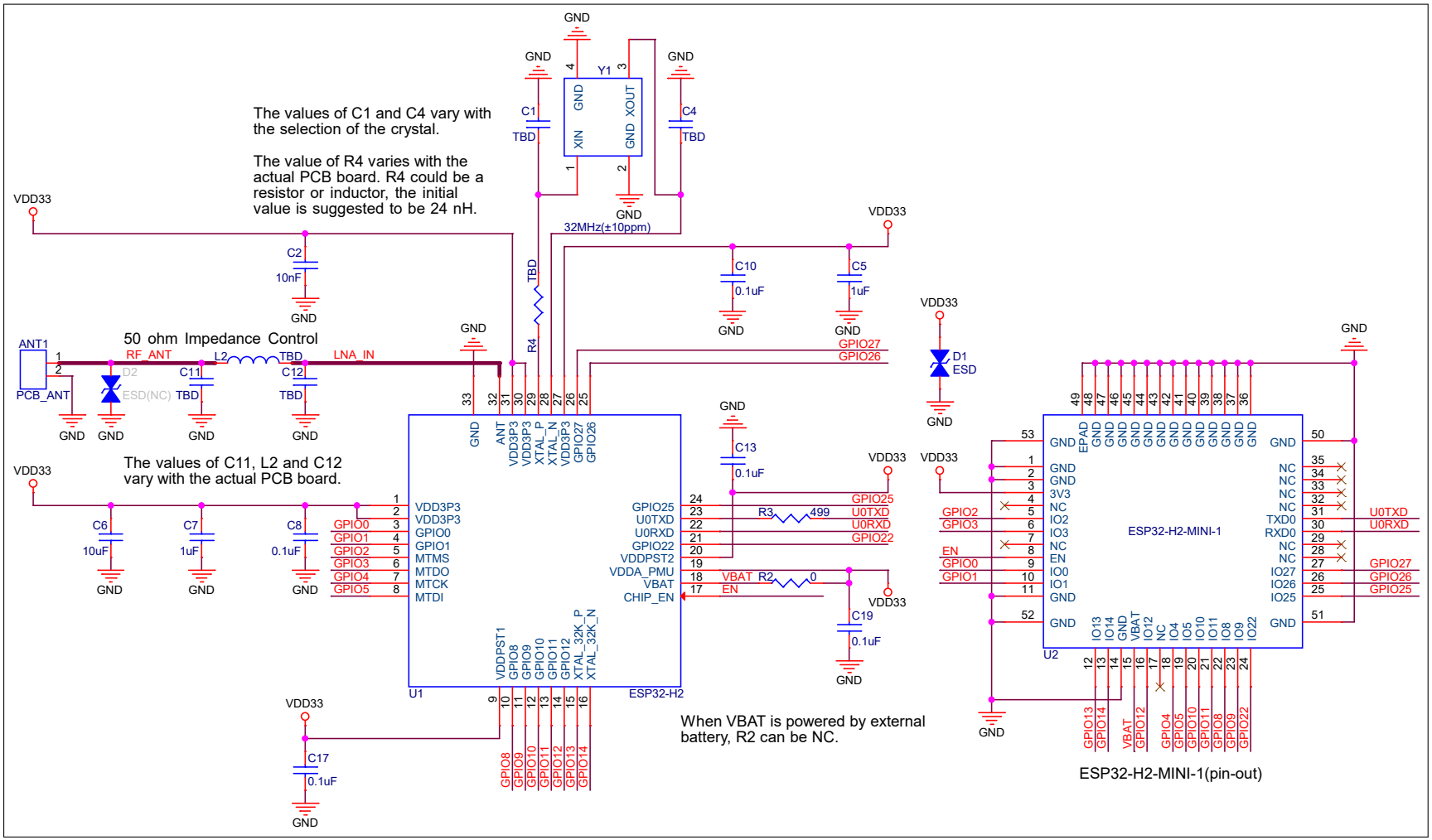

Figure 5: ESP32-H2-MINI-1 Schematics

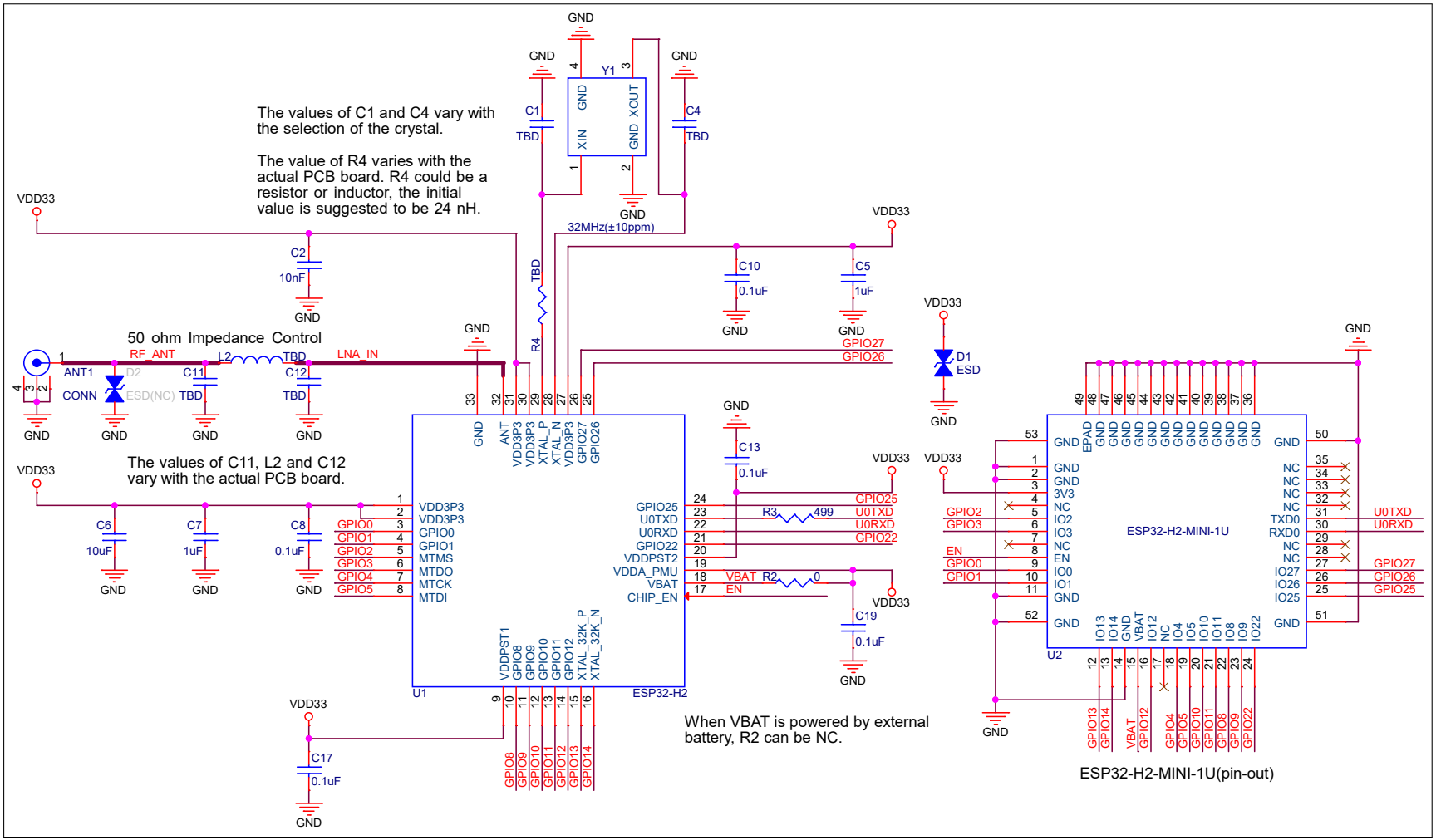

Figure 6: ESP32-H2-MINI-1U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

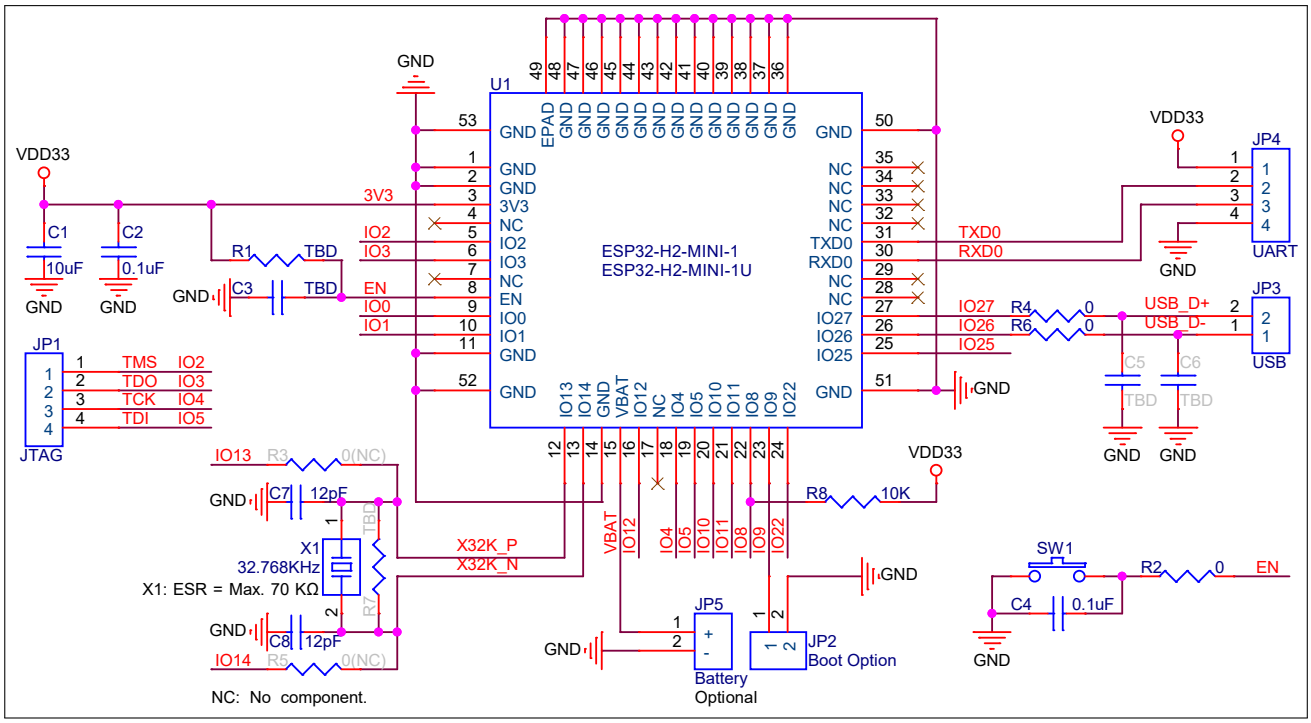

Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-H2 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-H2's power-up and reset sequence timing diagram, please refer to *ESP32-H2 Series Datasheet* > Section *Power Supply*.

10 Physical Dimensions

10.1 Module Dimensions

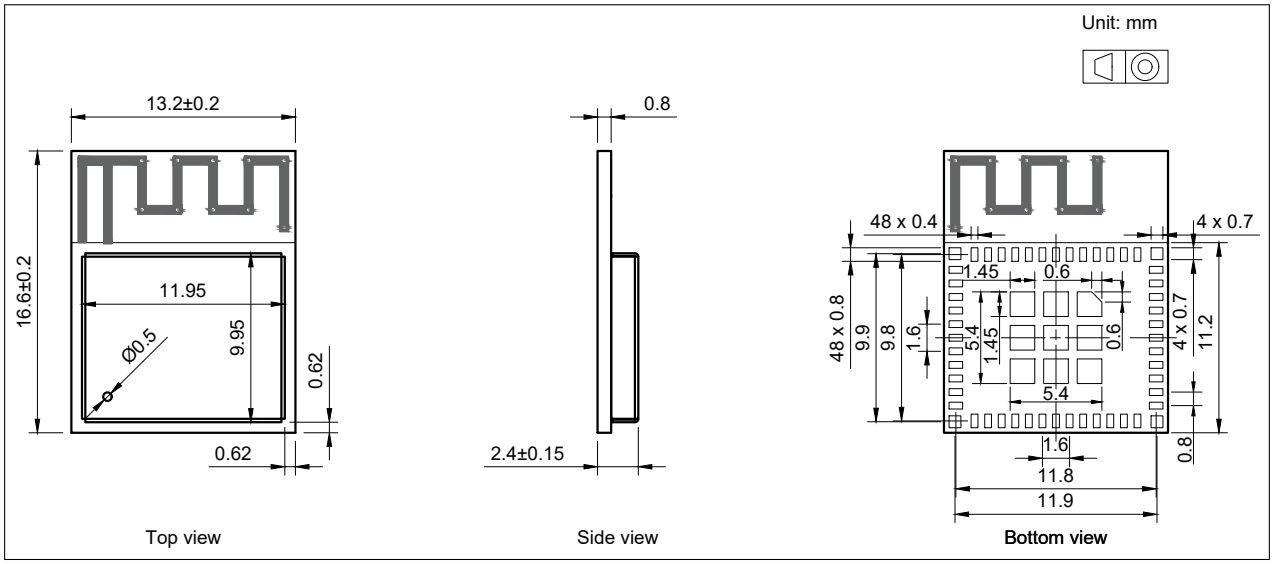

Figure 8: ESP32-H2-MINI-1 Physical Dimensions

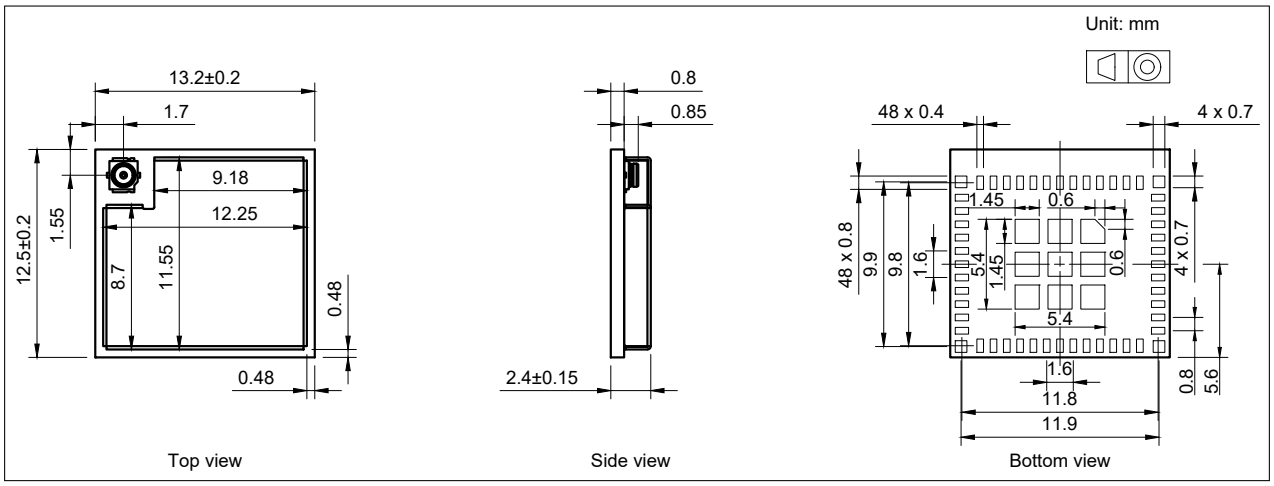

Figure 9: ESP32-H2-MINI-1U Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *Espressif Module Packaging Information*.

10.2 Dimensions of External Antenna Connector

ESP32-H2-MINI-1U uses the third generation external antenna connector as shown in Figure 10 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- W.FL Series connector from Hirose
- MHF III connector from I-PEX
- AMMC connector from Amphenol

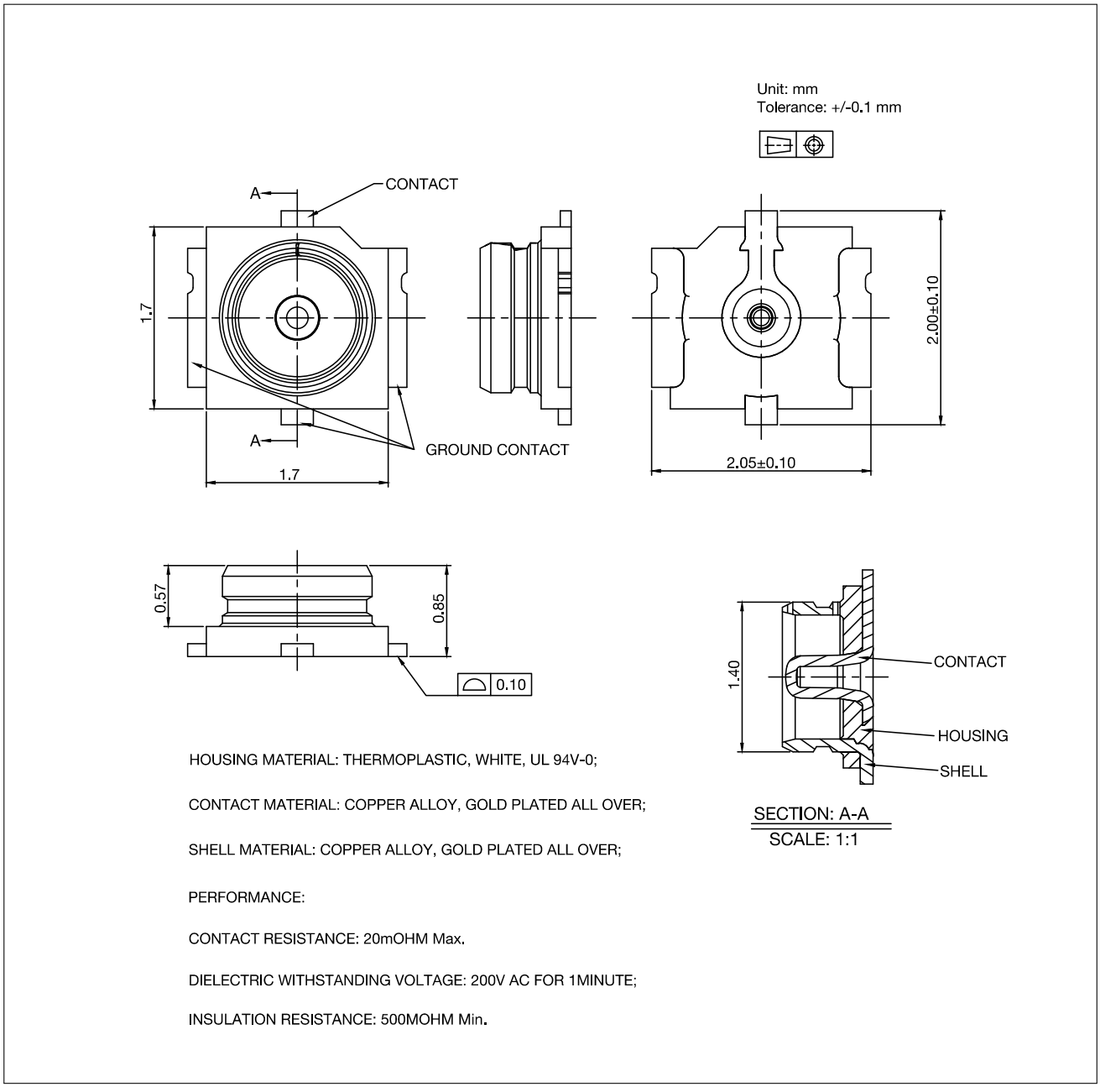

Figure 10: Dimensions of External Antenna Connector

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figure 11 *ESP32-H2-MINI-1 Recommended PCB Land Pattern* and Figure 12 *ESP32-H2-MINI-1U Recommended PCB Land Pattern*: the recommended PCB land patterns with all the dimensions needed for PCB design.
- Source files for ESP32-H2-MINI-1 and ESP32-H2-MINI-1U: the recommended PCB land patterns to measure dimensions not covered in Figure 11 and Figure 12. You can view the source files with Autodesk Viewer.
- 3D models of ESP32-H2-MINI-1 and ESP32-H2-MINI-1U: the .STEP format file. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

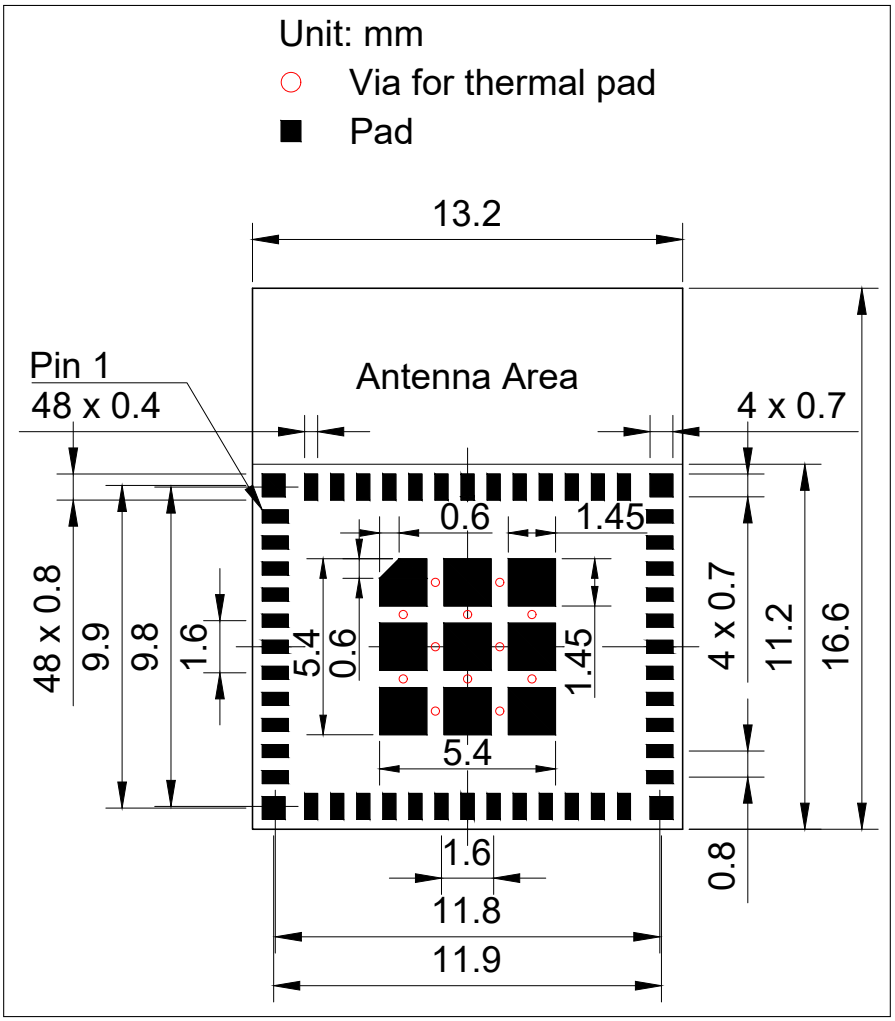

Figure 11: ESP32-H2-MINI-1 Recommended PCB Land Pattern

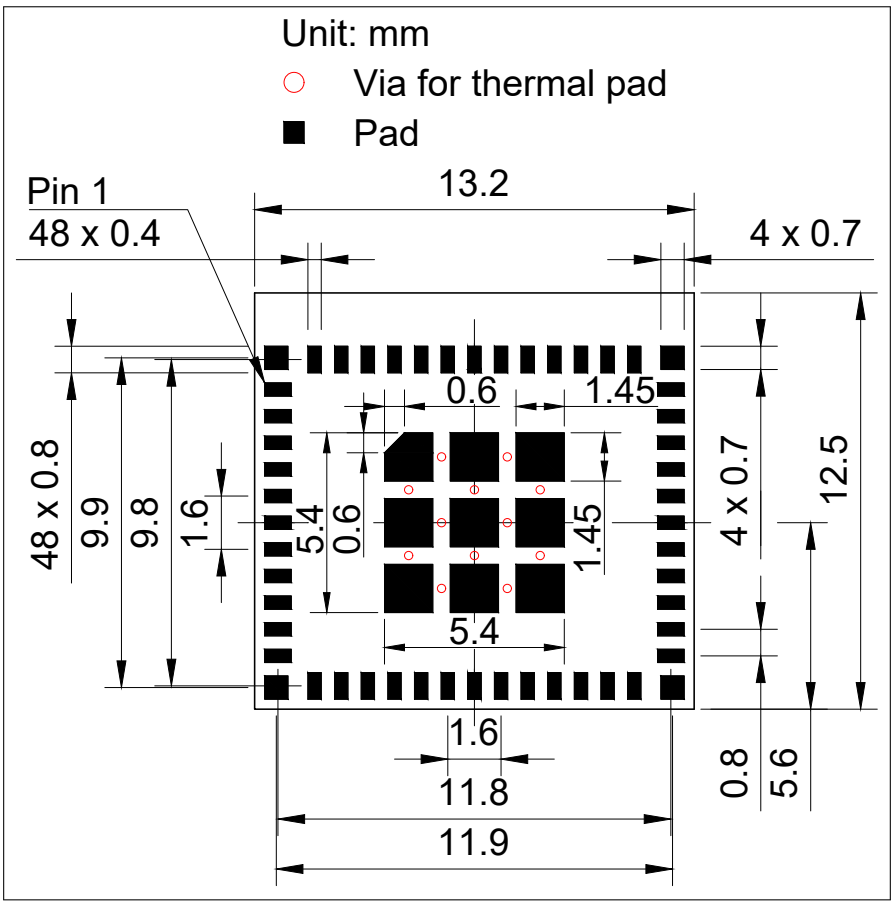

Figure 12: ESP32-H2-MINI-1U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-H2 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Soldering Profile

12.3.1 Reflow Profile

Solder the module in a single reflow.

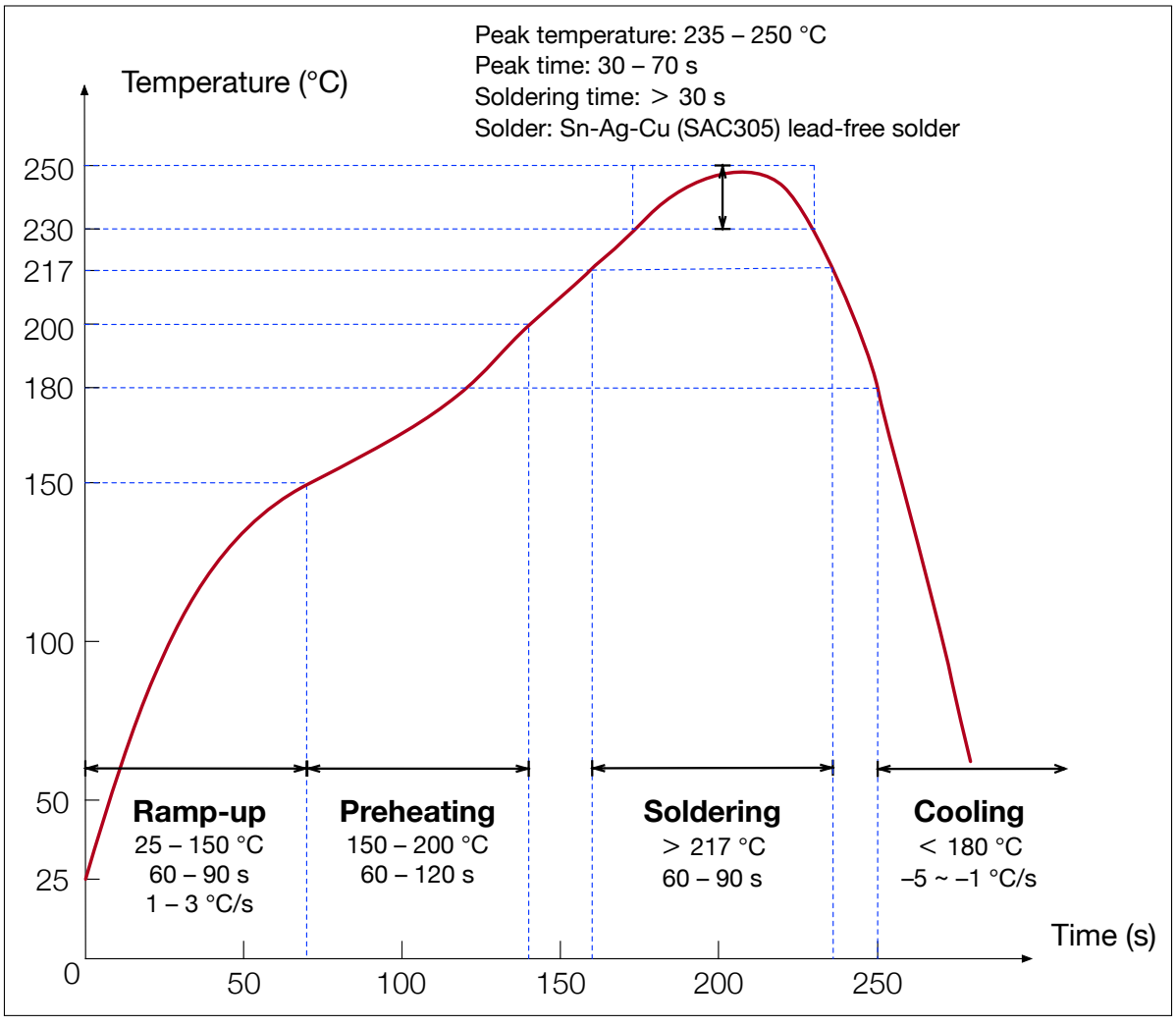

Figure 13: Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Related Documentation and Resources

Related Documentation

- ESP32-H2 Series Datasheet – Specifications of the ESP32-H2 hardware.
- ESP32-H2 Technical Reference Manual – Detailed information on how to use the ESP32-H2 memory and peripherals.
- ESP32-H2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-H2 into your hardware product.
- ESP32-H2 Series SoC Errata – Descriptions of known errors in ESP32-H2 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-H2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-H2
- *ESP32-H2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-H2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-H2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-H2 Series SoCs* – Browse through all ESP32-H2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-H2
- *ESP32-H2 Series Modules* – Browse through all ESP32-H2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-H2
- *ESP32-H2 Series DevKits* – Browse through all ESP32-H2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-H2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2025-05-06	v1.2	Updated Table 17 and Table 27
2025-02-28	v1.1	Updated the ordering code in Section 1.2 *Series Comparison* according to chip revision v1.2
2024-11-08	v1.0	• Official release • Improved the content, formatting, structure, and wording of the whole document
2023-10-17	v0.6	• Updated the description about Boot Mode Control in Section *Strapping Pins*. • Updated the descriptions about resources offered in Section 11.1 *PCB Land Pattern*. • Updated measurements in Table 15 and 16.
2023-05-24	v0.5	Preliminary release

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